IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 3838
Hiroki Goko	)	Examiner: MEMULA, Suresh
Application No. 10/813,031	)	Group Art Unit: 2825
Filed: March 31, 2004	)	
For: APPARATUS AND METHOD FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT	)	Date: January 21, 2010

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
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Sir:

INTRODUCTORY COMMENTS

This is an appeal brief filed pursuant to the Notice of Appeal filed October 28, 2009 and to the final Office Action dated April 28, 2009, in which claims 1-5 are rejected in the above-identified application.

I. REAL PARTY OF INTEREST

The real party of interest is the assignee of record: OKI Electric Industry Co., LTD (Tokyo, JAPAN).

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

A. Status of Claims in Proceeding

Claims 1-5 are currently pending in the application.

B. Identification of Appealed Claims

Claims 1-5 are being appealed. A copy of all of the pending claims as presented in the last entered amendment dated January 13, 2009 is included in the attached Appendix I.

IV. STATUS OF AMENDMENTS

There are no pending amendments of the claims. The last communication prior to the Pre-Appeal Brief Request for Review was the Request for Reconsideration filed on July 28, 2009 of which entry was acknowledged in the Advisory Action dated August 14, 2009.

Claims 1-5 are pending.

V. SUMMARY OF CLAIMED SUBJECT MATTER

For the purposes of appeal, the rejection of independent claim 1 and its dependent claims 2-5 is appealed. The dependent claims do not stand or fall together with their respective independent claim.

Claim 1 is directed to a method of designing a semiconductor integrated circuit, comprising a first step (Fig. 3, substep SS16 and lines 24-25 in page 13 of the specification) for determining a number of clocks different in delay amount, which are used for verification of a circuit design of the semiconductor integrated circuit upon the circuit design thereof, and determining delays in the clocks on the basis of pre-set conditions for constraints of timings;

a second step (Fig. 3, substep SS20 and line 9 in page 14 of the specification) for allocating clocks supplied to respective circuits, and

a third step (Fig. 3, substep SS22 and line 2 in page 18 of the specification) for optimizing timings on the basis of a list obtained by the timing constraint conditions and the clock allocation, and determining whether results of analyses of the respective timings correspond to violation of the constraints of timings,

wherein the optimization of the timings is repeated (Fig. 3, substep SS24 and lines 10-12 in page 18 of the specification) according to the violation of the constraints of timings and the first, second, and third steps are directed to circuit design and are(SUB1 in Fig. 3) performed prior to performing a layout design (SUB2 in Fig. 4) of the semiconductor integrated circuit.

Claim 2 is directed to a method according to claim 1, further comprising performing a layout design (SUB2 in Fig. 4) including a fourth step (Fig. 4, substep SS34 and line 1, page 19 of the specification) for generating the clocks different in the delay amount for the verification of a layout design of the semiconductor integrated circuit,

a fifth step (Fig. 4, substep SS36 and line 5, page 19 of the specification) for adjusting skews for each of said clocks;

a sixth step (Fig. 4, substep SS38 and line 9, page 19 of the specification) for

adjusting delays respectively included in the clocks to the determined clock delays upon the layout design, respectively, and

a seventh step (Fig. 4, substep SS40 and line 11, page 19 of the specification) for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design and determining whether analytical results of the respective timings correspond to the constraint violation,

wherein the layout adjustment is repeated according to the constraint violation.

Claim 3 is directed to a method according to claim 1, further comprising a step (SS28 in Fig. 8 and lines 1-23 in page 21 of the specification) for adjusting the delay of each of the clocks again according to the constraint violation when the constraint violation exists in the third step.

Claim 4 is directed to a method according to claim 2, further comprising a step (Fig. 8, substep SS46) for adjusting delays set for said clocks according to the constraint violation when the constraint violation occurs in the seventh step.

Claim 5 is directed to a method according to claim 4, wherein adjusting the delays comprises adding a delay at a starting point where data is outputted, and determining the clock delays according to the difference between the added value and the cycle of the clock (lines 8-18 in page 23 of the specification).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-5 stand rejected under 35 U.S.C. §102(e) as being anticipated by Weaver, Jr. (US 2004/0230933 – hereinafter Weaver).

VII. ARGUMENT

As discussed in detail below, the basis for the rejection of claims 1-5 does not amount to a case of anticipation for the combination of subject matter recited in the rejected claims.

1. Claim Rejections under 35 U.S.C. §102(e)

Claims 1-5 were rejected under 35 U.S.C. §102(e) as being anticipated by *Weaver, Jr.* (US 2004/0230933 – hereinafter *Weaver*).

A. Pertinent Law

As set forth in the MPEP, "to anticipate a claim, the reference must teach every element of the claim." (MPEP §2131). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

B. The *Weaver* patent does not anticipate claims 1-5

Reversal of the rejection of claims 1 - 5 is respectfully requested on the basis that *Weaver* fails to describe of each and every element recited in claims 1-5.

According to the present invention, a method of designing semiconductor ICs comprises two separate routines, a circuit design routine and a layout design routine, as shown in Fig. 2 of the application. The circuit design routine is the first routine SUB1, and following the circuit design routine is a layout design routine SUB2.

Claim 1 is directed to the circuit design routine SUB1, which is shown in detail as substeps (e.g., SS16, SS20, SS22, and SS24) in Fig. 3, while dependent claim 2 is directed to the sequential layout design routine SUB2 shown in detail as substeps (e.g., SS34, SS36, SS38, SS40, and SS42) in Fig. 4.

The steps for circuit design routine in SUB1 in Fig. 3 are performed before the steps in the layout design routine SUB2 in Fig. 4. Hence, the claimed steps 1st through 7th steps in claims 1 and 2 are performed in proper order as recited in the claims.

With Appellant's claimed method as recited in the steps of claims 1 and 2, for example, timing analysis is performed using the plural clocks even in the layout design (i.e., SUB2 steps) to make a decision as to whether violation of timing constraints has occurred, thereby making it possible to obtain a layout design that has satisfied all constraints, as discussed in lines 3-8 in page 20 of the specification.

In contrast with Appellant's claimed invention, Weaver generally describes an IC design methodology that applies manual pre-placement (i.e., layout) of certain critical circuit elements followed by circuit optimization based on timing estimates at an early stage in the design process. According to paragraph [0045] of Weaver, after the circuit design phase, the placed netlist (i.e., designed and optimized circuit) may be provided to a layout vendor, who may then perform a full layout design of the completed design and optimized netlist. That is, Weaver is directed mainly to a design process with manual pre-placement of certain critical circuit elements at an early stage in the circuit design process, while leaving the main layout process to be performed by a layout vendor. Hence, Weaver does not follow the sequential or even logical order nor include the combination of steps recited in claim 1 directed to a design process.

In the rejection of claim 1, the Examiner contends that Appellant's claimed 2nd step for allocating clocks supplied to respective circuit is anticipated by Weaver's "element 6". That is, as contended by the Examiner, "element 6" of Weaver is interpreted as a circuit design step and not a layout design step. However,

such an interpretation is contrary to the teachings of Weaver at least for the reasons explained below.

Appellant's claimed 2nd step in a method of designing semiconductor ICs that includes two separate routines. As shown in Fig. 2 of the application, the 2nd step is a part of a first routine SUB1, which is a circuit design routine. As mentioned previously, according to the claimed invention, following the completion of the circuit design routine (i.e., SUB1) is a layout design routine (i.e., SUB2).

In contrast with Appellant's 2nd step in the design routine, Weaver's "element 6" is related to the pre-placement (i.e., layout) of critical electrical infrastructure (i.e., physical system layout). According to Weaver, "element 6" performing a pre-placement or layout design step is an unconventional step in the midst of a circuit design phase, which begins in block 2 in Fig. 1 of Weaver.

Further, in Weaver there is "element 8" that provides a repeat of the pre-placement process 6 based on the condition of whether congestion is acceptable or not. This conditional repeat does not exist in Appellant's 2nd step. Therefore, Appellant respectfully submits that there is no claimed step in the present invention that remotely suggests or is equivalent to the manual pre-placement of critical electrical infrastructure in "element 6" of Weaver.

With respect to claim 2, since Weaver's IC design method includes a pre-placement of critical circuit elements in a circuit design process followed by circuit optimization based on timing estimates at an early stage in the design process, and since Weaver clearly states that layout design may be performed separately by a layout vendor, it is logical that Weaver also does not disclose the features of a layout design process recited in claim 2 in Appellant's claimed invention.

More specifically, as described in, e.g., paragraph [0014] of Weaver, the pre-placement process may involve locating and fixing strategic electrical infrastructure such as clock trees, ESD protection circuits, I/O circuit, etc., followed by automatic placement (i.e., layout) of the remainder of the chip circuits. The methodology of

Weaver with pre-placement of critical electrical infrastructure (i.e., physical system layout) prior to a design phase is shown in the single drawing Fig. 1 of Weaver.

Moreover, Appellant respectfully notes, e.g., paragraph [0034] of Weaver describing the pre-placement (i.e., layout) step in a circuit synthesis/design that begins in block 2 and continues in, e.g., block 10 and thereafter.

Further, according to Weaver's paragraph [0014], employing a layout design step (i.e., pre-placement of critical circuits) in an early stage of a circuit design phase is advantageous because the predictability of results is improved. That is, by performing a layout step (i.e., block 6) during the circuit design phase, problems with the critical components placement can be detected and solved early in circuit design. Thus, when a completed circuit design is provided to a layout vendor for a full layout, less problems and less redesign of circuit can be expected. As clearly recited in Appellant's claim 1 directed to a design process, there is no pre-placement or layout steps as required by Weaver's teachings.

Still further, in the rejection of claim 2, the Examiner contends that "element 18", which is performed after the design process shown in elements 4, 6, 10, 14, and 16, corresponds to Appellant's layout sign process. However, Weaver specifically labels "element 18" as "route and parasitic extraction", which precedes "static timing analysis" block 20 in Weaver. Appellant respectfully asserts that there is no relationship between the "static timing analysis" block 20 of Weaver to Appellant's 4th step for generating clocks different in delay amount for the verification of a layout design.

Further, although Weaver shows a decision block 22 determining whether or not timing is met, there is no disclosure of adjusting skews and adjusting delays, as recited in Appellant's 5th and 6th steps, respectively.

Still further, the Examiner contends that "elements 10 and 22" of Weaver are equivalent to Appellant's 3rd step as well as the 5th and 6th steps. However, Appellant's 3rd step is not interchangeable or equivalent to the 5th and 6th step. Hence, such a contention by the Examiner is illogical and insupportable.

Appellant respectfully acknowledges that Examiners are entitled to interpreting a reference broadly. However, the reference's teaching may not be taken out of context such that its original functionality is misapplied, such as in the case of the improper application/interpretation of Weaver.

With respect to claim 3, as Weave fails to disclose Appellant's claimed step 3 as explained above, Weaver also fails to disclose a step (e.g., SS28 in Fig. 8 and lines 1-23 in page 21 of the specification) for adjusting the delay of each of the clocks again according to the constraint violation when the constraint violation exists in the third step recited in claim 3 of the present invention.

With respect to claim 4, as Weave fails to disclose Appellant's claimed step 7 as explained above, Weaver also fails to disclose a step (e.g., substep SS46 in Fig. 8) for adjusting delays set for said clocks according to the constraint violation when the constraint violation occurs in the seventh step of the presently claimed invention.

With respect to claim 5, as Weave fails to disclose the features of claim 4, it follows that Weaver also fails to disclose adjusting the delays comprises adding an delay at a starting point where data is outputted, and determining the clock delays according to the difference between the added value and the cycle of the clock (see lines 8-18 in page 23 of the specification) as recited in claim 5 of the present invention.

In view of the arguments set forth above, each and every feature of the present claims is not taught (and is not inherent) in Weaver, as is required by MPEP Chapter 2131 in order to establish anticipation. Hence, the rejection of claims 1-5, under 35 U.S.C. §102(e), as anticipated by Weaver is improper.

Reconsideration and withdrawal of the rejection of claim 1-5, in view of clear errors in the Final Office Action, is respectfully requested.

VIII. Conclusion

For the reasons set forth above, claims 1-5 of the pending application define subject matter that is not anticipated under 35 U.S.C. § 102(e) in view of the *Weaver*. Accordingly, reversal of the rejection of claims 1-5 is respectfully requested.

Further, while no fees are believed to be due, the Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-4525.

Respectfully submitted,

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IX. CLAIMS APPENDIX

1. A method of designing a semiconductor integrated circuit, comprising:

a first step for determining a number of clocks different in delay amount, which are used for verification of a circuit design of the semiconductor integrated circuit upon the circuit design thereof, and determining delays in the clocks on the basis of pre-set conditions for constraints of timings;

a second step for allocating clocks supplied to respective circuits; and

a third step for optimizing timings on the basis of a list obtained by the timing constraint conditions and the clock allocation, and determining whether results of analyses of the respective timings correspond to violation of the constraints of timings,

wherein the optimization of the timings is repeated according to the violation of the constraints of timings and the first, second, and third steps are directed to circuit design and are performed prior to performing a layout design of the semiconductor integrated circuit.

2. A method according to claim 1, further comprising performing a layout design including:

a fourth step for generating the clocks different in the delay amount for the verification of a layout design of the semiconductor integrated circuit;

a fifth step for adjusting skews for each of said clocks;

a sixth step for adjusting delays respectively included in the clocks to the determined clock delays upon the layout design, respectively; and

a seventh step for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design and determining whether analytical results of the respective timings correspond to the constraint violation,

wherein the layout adjustment is repeated according to the constraint violation.

3. A method according to claim 1, further comprising a step for adjusting the delay of each of the clocks again according to the constraint violation when the constraint violation exists in the third step.

4. A method according to claim 2, further comprising a step for adjusting delays set for said clocks according to the constraint violation when the constraint violation occurs in the seventh step.

5. A method according to claim 4, wherein adjusting the delays comprises adding an delay at a starting point where data is outputted, and determining the clock delays according to the difference between the added value and the cycle of the clock.

X. EVIDENCE APPENDIX

There are no copies of evidence entered and relied upon in this appeal of the pending application.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings or decisions rendered by a court or the Board of Appeals in any proceeding identified in the related appeals and interferences section in the pending application.